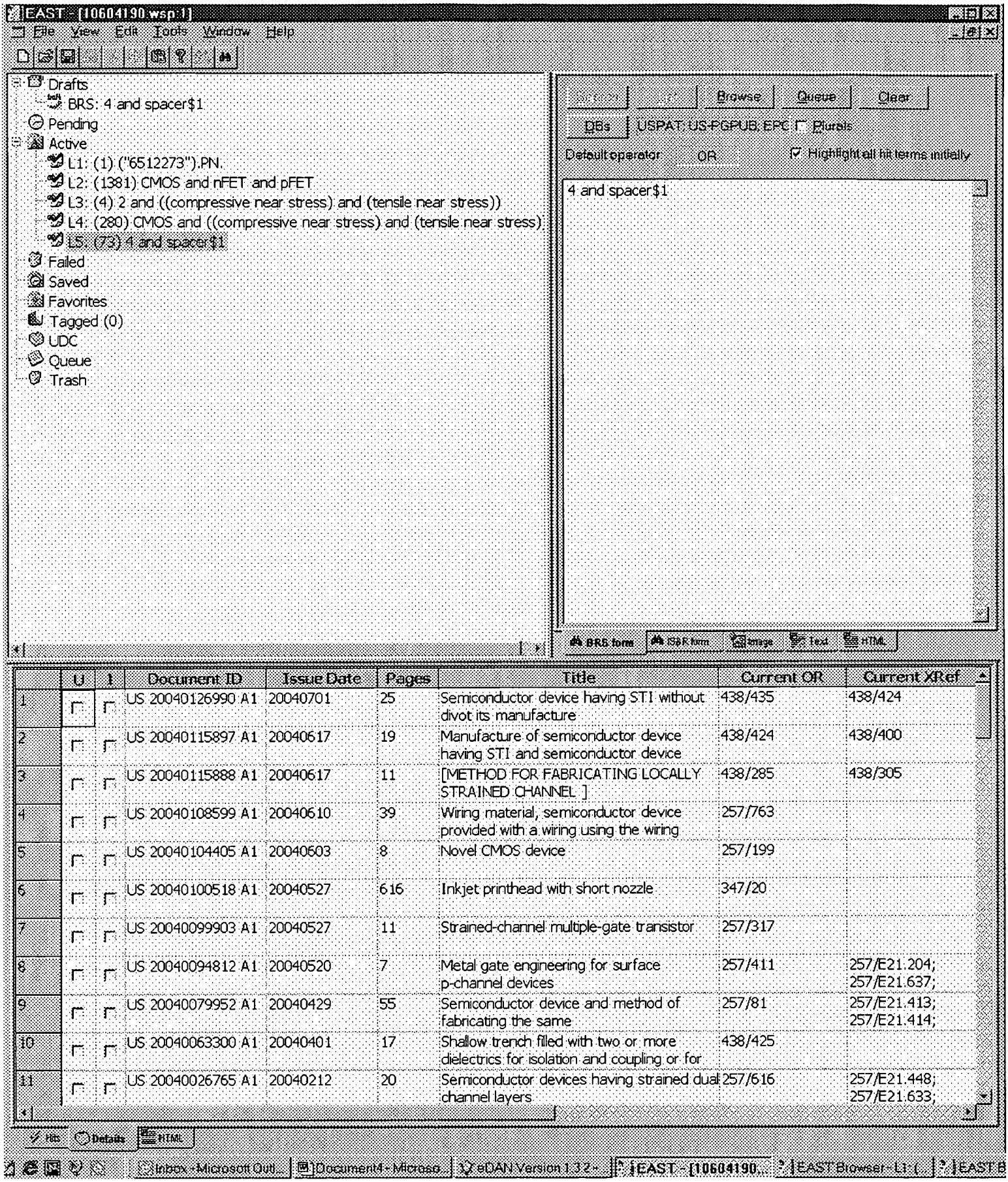
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Drafts
BRS: 4 and spacer$1
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L1: (1) ("6512273").PN.
L2: (1381) CMOS and nFET and pFET
L3: (4) 2 and ((compressive near stress) and (tensile near stress))
L4: (280) CMOS and ((compressive near stress) and (tensile near stress))
L5: (73) 4 and spacer$1
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4 and spacer$1
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1 US 20040126990 A1 20040701 25 Semiconductor device having STI without divot its manufacture 438/435 438/424
2 US 20040115897 A1 20040617 19 Manufacture of semiconductor device having STI and semiconductor device 438/424 438/400
3 US 20040115888 A1 20040617 11 [METHOD FOR FABRICATING LOCALLY STRAINED CHANNEL] 438/285 438/305
4 US 20040108599 A1 20040610 39 Wiring material, semiconductor device provided with a wiring using the wiring 257/763
5 US 20040104405 A1 20040603 8 Novel CMOS device 257/199
6 US 20040100518 A1 20040527 616 Inkjet printhead with short nozzle 347/20
7 US 20040099903 A1 20040527 11 Strained-channel multiple-gate transistor 257/317
8 US 20040094812 A1 20040520 7 Metal gate engineering for surface p-channel devices 257/411 257/E21.204; 257/E21.637;
9 US 20040079952 A1 20040429 55 Semiconductor device and method of fabricating the same 257/81 257/E21.413; 257/E21.414;
10 US 20040063300 A1 20040401 17 Shallow trench filled with two or more dielectrics for isolation and coupling or for 438/425
11 US 20040026765 A1 20040212 20 Semiconductor devices having strained dual channel layers 257/616 257/E21.448; 257/E21.633;
Hits
Details
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EAST B